QUALCOMM® QUICK CHARGE™ 3.0 TECHNOLOGY

CERTIFICATION TEST REPORT

FOR

AC ADAPTER

MODEL NUMBER: GW-UCS612

REPORT NUMBER: 4788284150-1

ISSUE DATE: February 1, 2018

Prepared for
HAPPYNOVA INC.
MANSURO 50 - 19, NAMDONGGU,
INCHEON, KR 21526

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Revision History

Rev.	Issue Date	Revisions	Revised By
--	2/1/2018	Initial Issue	D. Chiang

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1. ATTESTATION OF TEST RESULTS

COMPANY NAME: HAPPYNOVA INC.
MANSURO 50 - 19, NAMDONGGU,
INCHEON, KR 21526

EUT DESCRIPTION: AC ADAPTER

MODEL: GW-UCS612

SERIAL NUMBER: Prototype

DATE TESTED: January 24, 2018

APPLICABLE STANDARDS	
STANDARD	**TEST RESULTS**
High Voltage Dedicated Charging Port Interface Specification Revision K	Pass

UL Taiwan Co., Ltd. tested the above equipment in accordance with the requirements set forth in the above standards. All indications of Pass/Fail in this report are opinions expressed by UL Taiwan Co., Ltd. based on interpretations and/or observations of test results. Measurement Uncertainties were not taken into account and are published for informational purposes only. The test results show that the equipment tested is capable of demonstrating compliance with the requirements as documented in this report.

Note: The results documented in this report apply only to the tested sample, under the conditions and modes of operation as described herein. This document may not be altered or revised in any way unless done so by UL Taiwan Co., Ltd. and all revisions are duly noted in the revisions section. Any alteration of this document not carried out by UL Taiwan Co., Ltd. will constitute fraud and shall nullify the document. This report must not be used by the client to claim product certification, approval, or endorsement by Qualcomm.

Approved & Released For
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2. TRADEMARK NOTICES

Qualcomm is a trademark of Qualcomm Incorporated, registered in the United States and other countries. Qualcomm Quick Charge is a trademark of Qualcomm Incorporated. All Qualcomm Incorporated marks are used with permission.

3. TEST METHODOLOGY

The tests documented in this report were performed in accordance with High Voltage Dedicated Charging Port HVDCP Compliance Plan Revision D as amended by instructions from Qualcomm.

4. FACILITIES AND ACCREDITATION

The test sites and measurement facilities used to collect data are located at 5th Fl., 35, Sec. 2, Chungyang S. Road, Peitou District, Taipei City, Taiwan 112.

UL Taiwan Co., Ltd. is accredited by Taiwan Accreditation Foundation (TAF), Laboratory Code 0944. The full scope of accreditation can be viewed at http://hr.taftw.org.tw/service/labinfoE.aspx?code=0944.

Notes:

1. All measurements documented in this report are outside the scope of the Laboratory's TAF accreditation.
2. The Laboratory used for performing the measurements documented in this report is third party accredited to ISO 17025.

5. CALIBRATION AND UNCERTAINTY

5.1. MEASURING INSTRUMENT CALIBRATION

The measuring equipment utilized to perform the tests documented in this report has been calibrated in accordance with the manufacturer's recommendations, and is traceable to recognized national standards.

5.2. TEST AND MEASUREMENT EQUIPMENT

The following test and measurement equipment was utilized for the tests documented in this report:

TEST EQUIPMENT LIST					
Description	**Manufacturer**	**Model**	**Asset**	**Cal Date**	**Cal Due**
SourceMeter SMU instrument	KEITHLEY	2606B	85188	2017/5/16	2018/5/31
Oscilloscope	LeCroy	HDO6034	85085	2017/4/13	2018/4/30
Multimeter	Agilent (Keysight)	U1241B	79608	2017/1/18	2018/1/31
DC Electronic Load Mainframe	CHROMA	63600-2	125204	2017/4/26	2018/4/30

6. EQUIPMENT UNDER TEST

6.1. DESCRIPTION OF EUT

The EUT is a QUALCOMM® Quick Charge™ 3.0 charger.

Input power is furnished by 100-240 Volt, 50-60 Hz AC mains supply.

The rated output current at each output voltage is as follows:

Output Voltage (Volts)	Rated Current (Amps)
5	3.0
9	2.0
12	1.5

HVDCP detection is performed by a separate interface IC.

The chipsets performing the HVDCP detection is U7: Fitipower, FP6601Q.

The Quick Charge output is furnished via a USB Type A connector.

7. TEST RESULTS

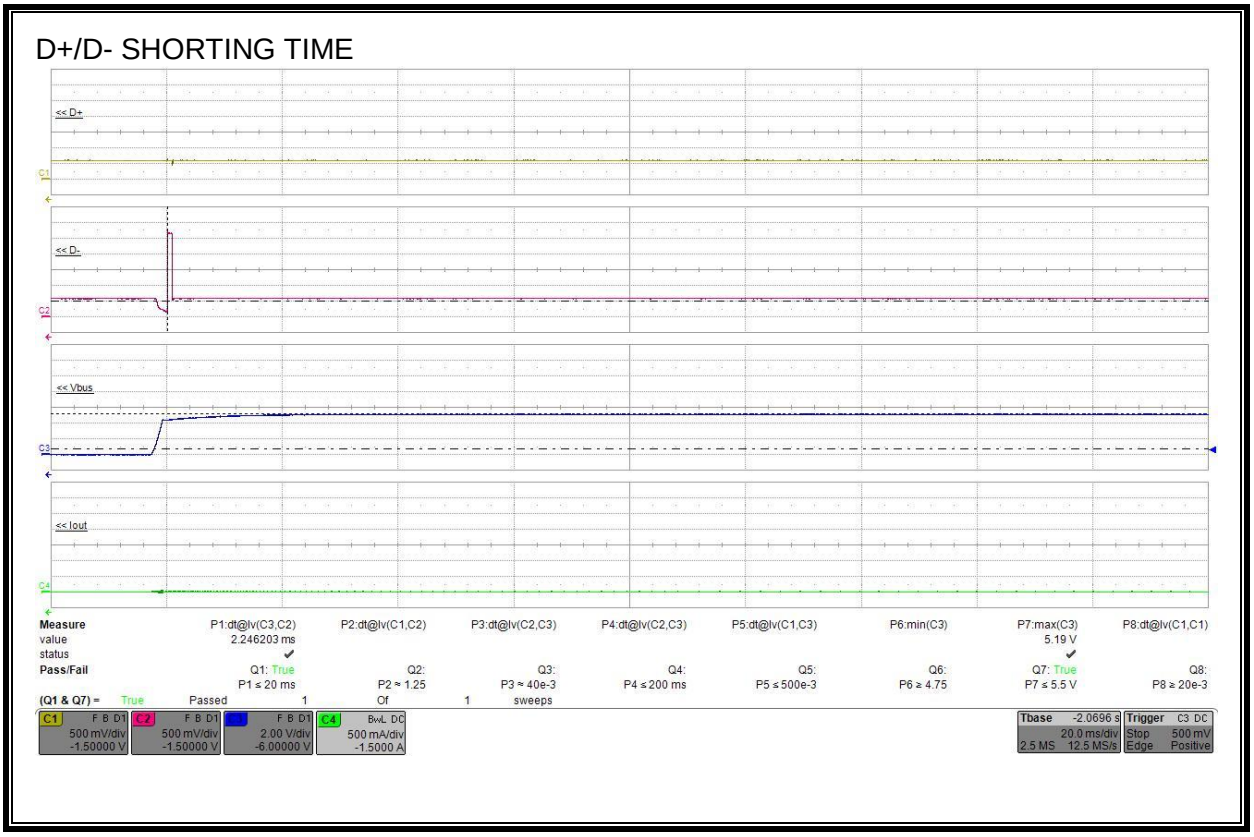
7.1. HVDCP Insertion

7.1.1. D+/D- Shorting Time

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Measured Value (ms)	Maximum Limit (ms)	Pass/Fail
Td+_d-_short	Vbus >= 0.8 V (Min Votg_sess_vld)	D- >= 0.5 V (Min Vdm_src)	2.246	20	PASS

WAVEFORM AND MEASUREMENTS



7.1.2. D+/D- Remains Shorted at 3.3 V

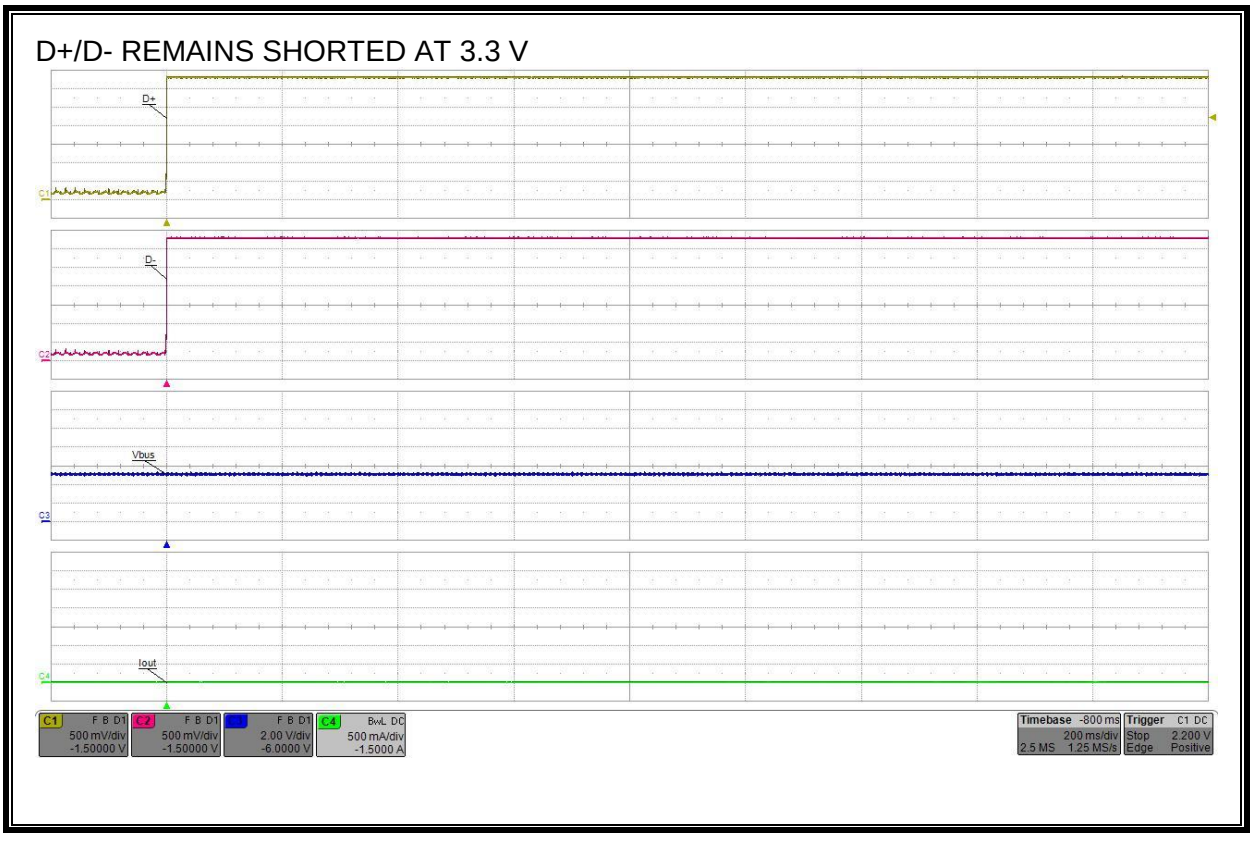
LIMITS AND RESULTS

Requirement: D- remains shorted to D+ when D+ is set to 3.3 V and D- Floats

Beginning 1.5 seconds (Max Tglitch_bc_done) after D+ >= 2.2 V (Max Vsel_ref), confirm D- >= 2.2 V (Max Vsel_ref)

Parameter	Measured Value (V)	Minimum Limit (V)	Pass/Fail
D-	3.30	2.2	PASS

WAVEFORM AND MEASUREMENTS



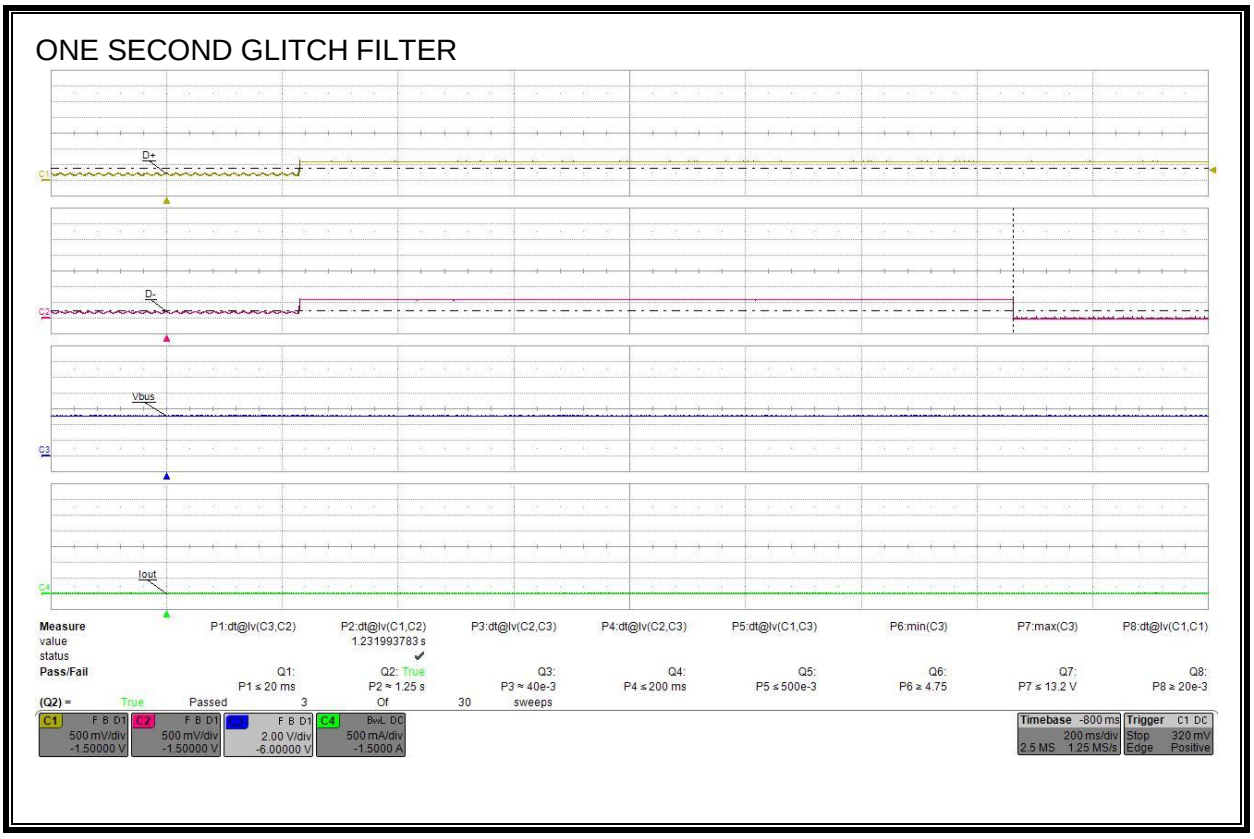
7.2. HVDCP Negotiation

7.2.1. One Second Glitch Filter

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Measured Value (s)	Minimum Limit (s)	Maximum Limit (s)	Pass/Fail
Tglitch_bc_done	D+ >= 0.4 V (Max Vdat_ref)	D- <= 0.25 V (Min Vdat_ref)	1.23	1.0	1.5	PASS

WAVEFORM AND MEASUREMENTS



7.2.2. Rdcp_dat

LIMITS AND RESULTS

Measured D+ Voltage (V)	Measured D- Voltage (V)	Measured D+ Current (mA)	Rdcp_dat Measured Value (ohms)	Rdcp_dat Maximum Limit (ohms)	Pass/Fail
0.600	0.592	0.988	8.1	40	PASS

7.2.3. Rdm_dwn

LIMITS AND RESULTS

Parameter	Measured Value (k ohms)	Minimum Limit (k ohms)	Maximum Limit (k ohms)	Pass/Fail
Rdm_dwn	20.860	14.25	24.80	PASS

7.2.4. Rdat_lkg

LIMITS AND RESULTS

Parameter	Measured Value (k ohms)	Minimum Limit (k ohms)	Maximum Limit (k ohms)	Pass/Fail
Rdat_lkg	561.4	300	1500	PASS

7.3. Portable Device Request Recognition

7.3.1. Output Voltage

LIMITS AND RESULTS

Output Voltage at No Load					
Nominal Vbus (V)	Load Current (A)	Measured Vbus (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
5	0.0	5.12	4.75	5.50	PASS
9	0.0	9.06	8.55	9.90	PASS
12	0.0	12.01	11.40	13.20	PASS

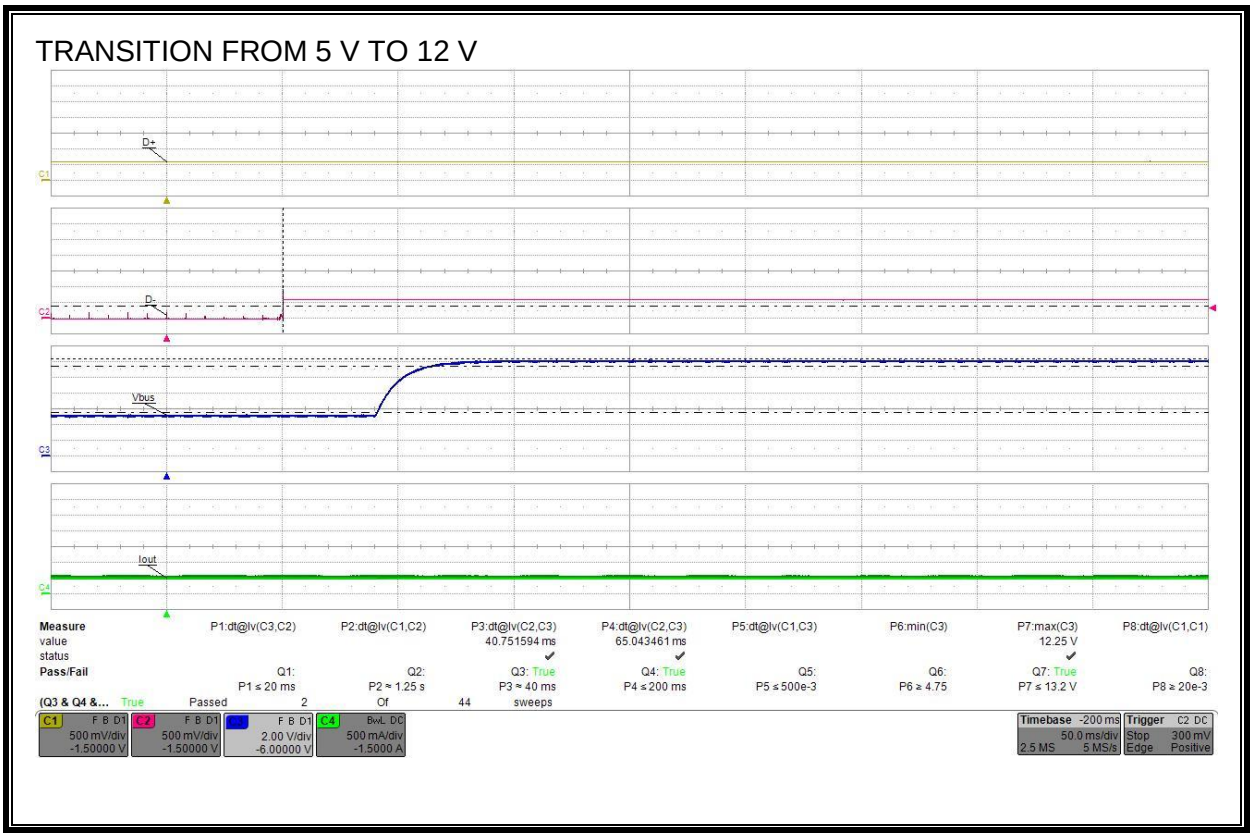
Output Voltage at Max Rated Load				
Nominal Vbus (V)	Load Current (A)	Measured Vbus (V)	Minimum Limit (V)	Pass/Fail
5	3.00	4.98	4.75	PASS
9	2.00	8.98	8.55	PASS
12	1.50	11.99	11.40	PASS

7.3.2. Transition from 5 V to 12 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 5.5 V (Max Vbus_5v)	40.75	20	60	PASS
Tv_new_request	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 11.4 V (Min Vbus_hv)	65.04		200	PASS

WAVEFORM AND MEASUREMENTS



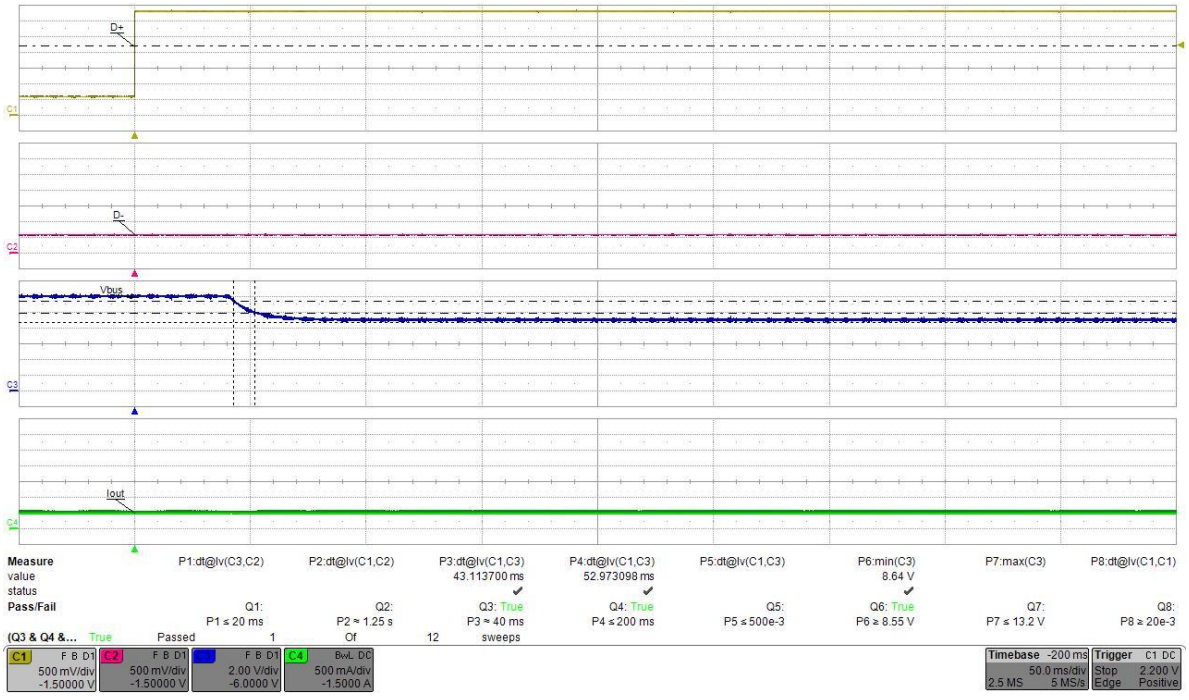
7.3.3. Transition from 12 V to 9 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 11.4 V (Min Vbus_hv)	43.11	20	60	PASS
Tv_new_request	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 9.9 V (Max Vbus_hv)	52.97		200	PASS

WAVEFORM AND MEASUREMENTS

TRANSITION FROM 12 V TO 9 V



7.3.4. Maintain 9 V with Reserved Request

LIMITS AND RESULTS

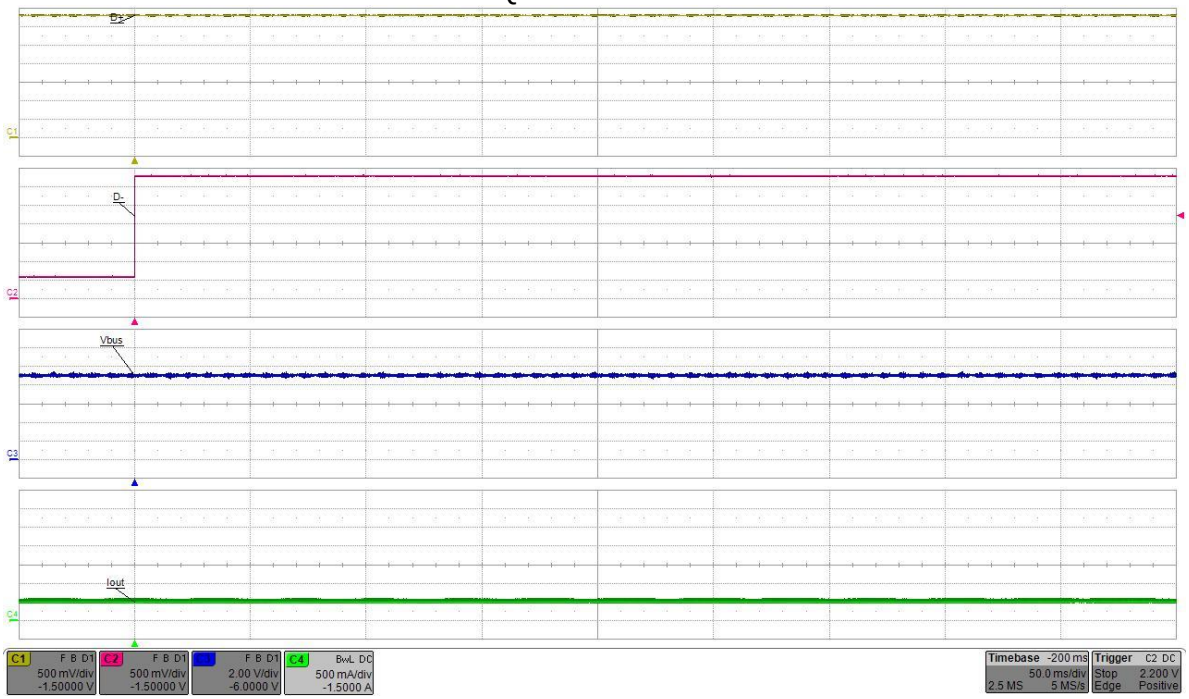
Initial Condition: Vbus is 9 volts

Observation Period: Monitor for longer than 200 ms (Max Tv_new_request) after Reserved Request is asserted

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
Vbus	9.053	8.55	9.90	PASS

WAVEFORM AND MEASUREMENTS

MAINTAIN 9 V WITH RESERVED REQUEST



7.3.5. Maintain 9 V with Continuous Request

LIMITS AND RESULTS

Initial Condition: Vbus is 9 volts

Observation Period: Monitor for longer than 200 ms (Max Tv_new_request) after Continuous Request is asserted

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
Vbus	9.053	8.55	9.90	PASS

WAVEFORM AND MEASUREMENTS

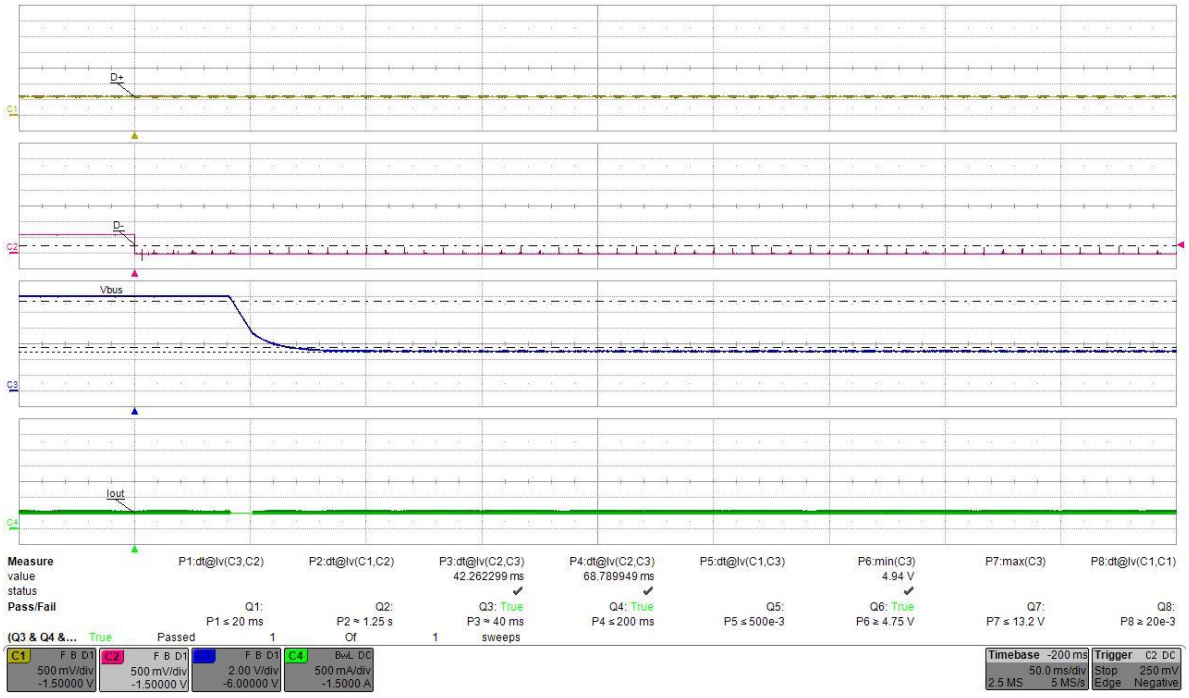
7.3.6. Transition from 12 V to 5 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- <= 0.25 V (Min Vdat_ref)	Vbus <= 11.4 V (Min Vbus_hv)	42.26	20	60	PASS
Tv_new_request	D- <= 0.25 V (Min Vdat_ref)	Vbus <= 5.5 V (Max Vbus_5v)	68.79		200	PASS

WAVEFORM AND MEASUREMENTS

TRANSITION FROM 12 V TO 5 V



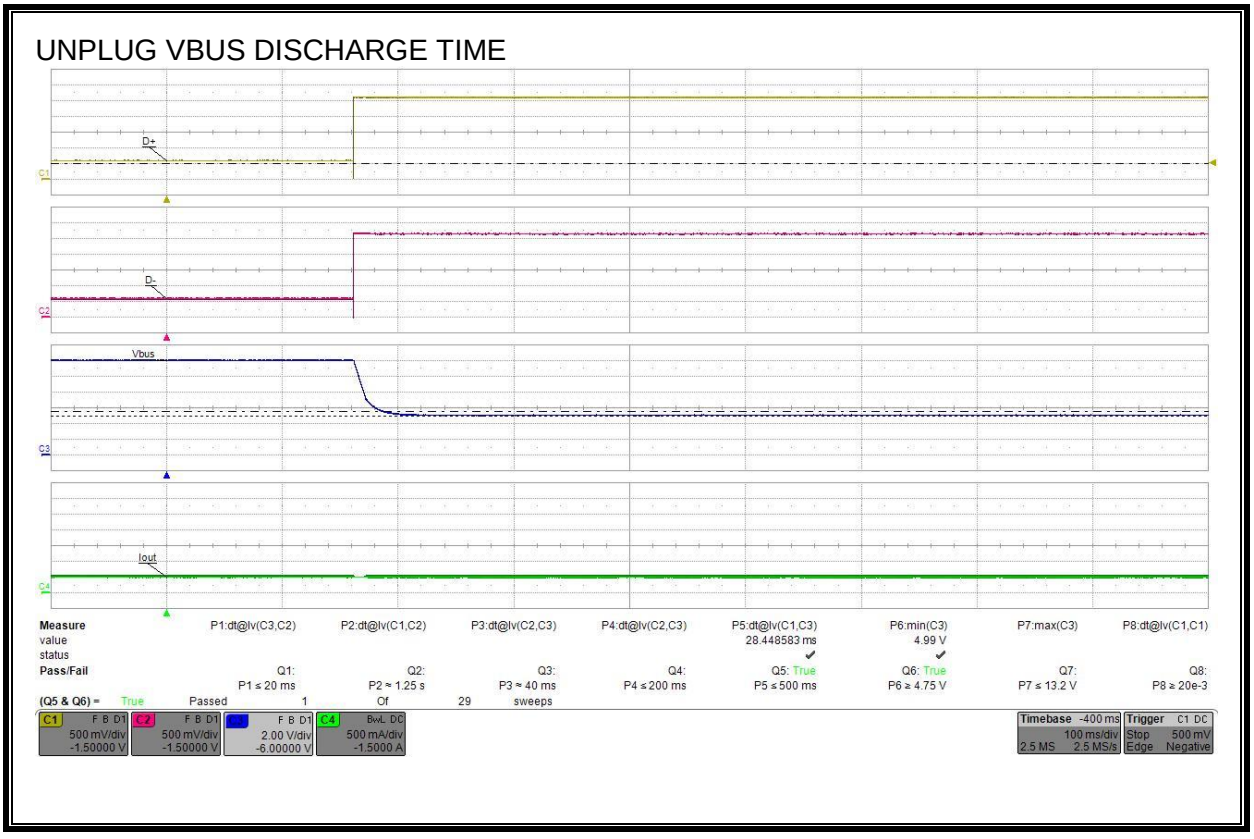
7.4. Portable Device Removal

7.4.1. Unplug Vbus Discharge Time

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Measured Value (ms)	Maximum Limit (ms)	Pass/Fail
Tv_unplug	D+ <= 0.5 V (Min Vdp_src)	Vbus <= 5.5 V (Max Vbus_5v)	28.45	500	PASS

WAVEFORM AND MEASUREMENTS



7.5. Portable Device USB PHY Error Rejection

7.5.1. Square Wave Error Rejection

LIMITS AND RESULTS

Initial Condition: Vbus is 5 volts
Applied Waveform: D+ = 0.6 V for 990 ms, then 0.6 V / 0 V pulse train, then remains at 0.6 V
Requirements: D- tracks D+ until Tglitch_bc_done after the completion of the pulse train, and Vbus remains at 5 volts
Observation Period: Monitor until at least 1.5 seconds after pulse train

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
D+/ D- Tracking				PASS
Vbus	5.100	4.75	5.50	PASS

WAVEFORM AND MEASUREMENTS

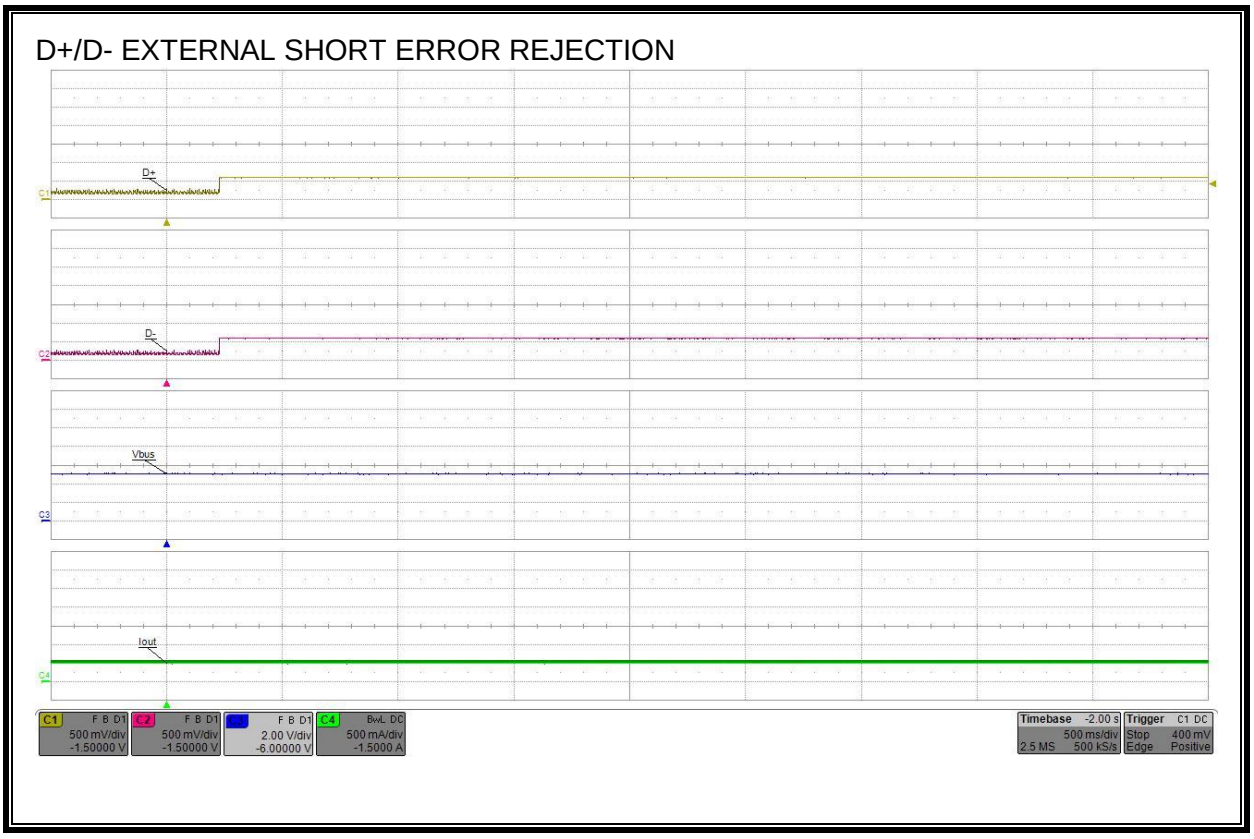
7.5.2. D+/D- External Short Error Rejection

LIMITS AND RESULTS

Initial Condition: Vbus is 5 volts
Applied Waveform: D+ and D- externally shorted together and held at 0 volts
Then 0.6 volts is applied to D+/D-
Requirement: Vbus remains at 5 volts
Observation Period: Monitor at least 2 seconds after 0.6 volts is applied

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
Vbus	5.099	4.75	5.50	PASS

WAVEFORM AND MEASUREMENTS



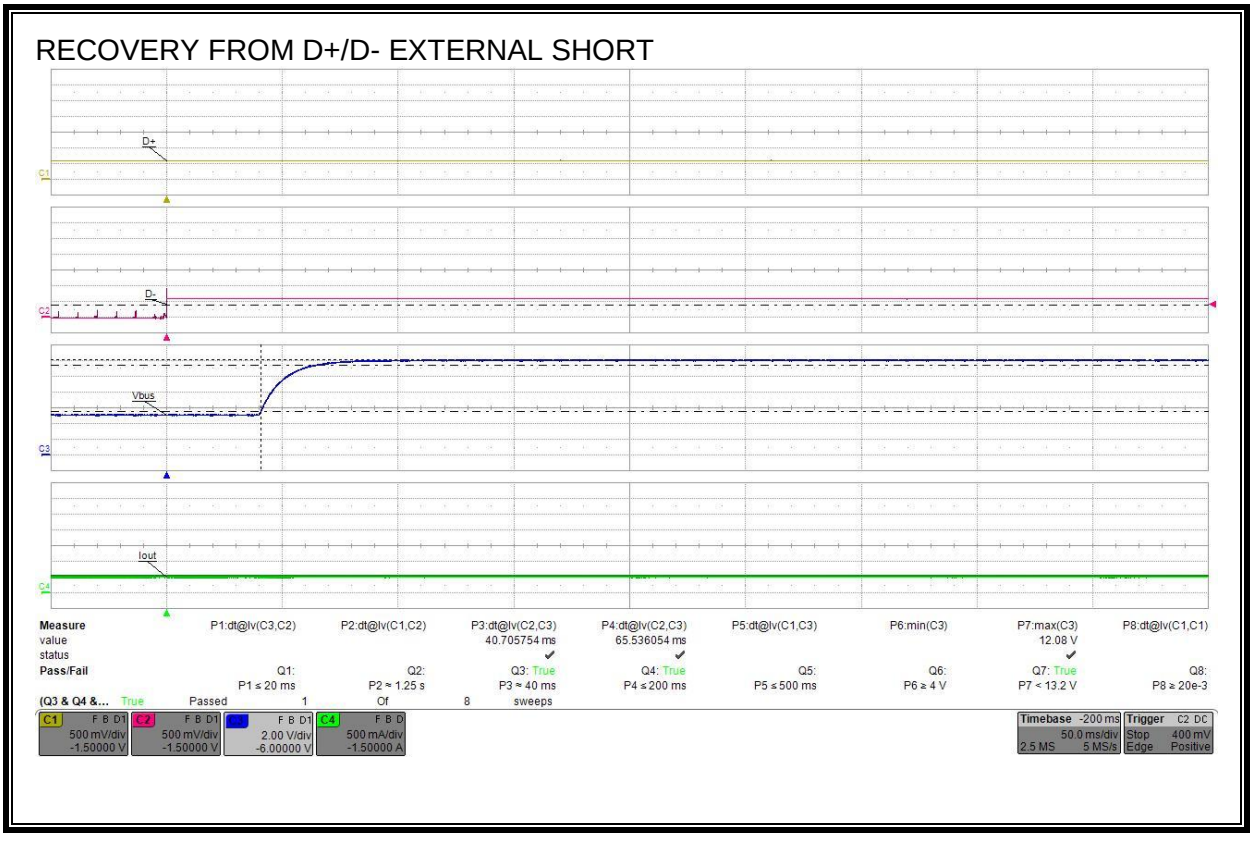
7.5.3. Recovery from D+/D- External Short

LIMITS AND RESULTS

Initial Condition: D+ and D- externally shorted together and held at 0.6 volts
Setup: Short is removed and D- allowed to float
Response: HVCDP asserts Rdm_dwn
Applied Waveform: 0.6 V is applied to D-
Requirement: Vbus makes a normal transition from 5 volts to 12 volts

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 5.5 V (Max Vbus_5v)	40.71	20	60	PASS
Tv_new_request	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 11.4 V (Min Vbus_hv)	65.54		200	PASS

WAVEFORM AND MEASUREMENTS



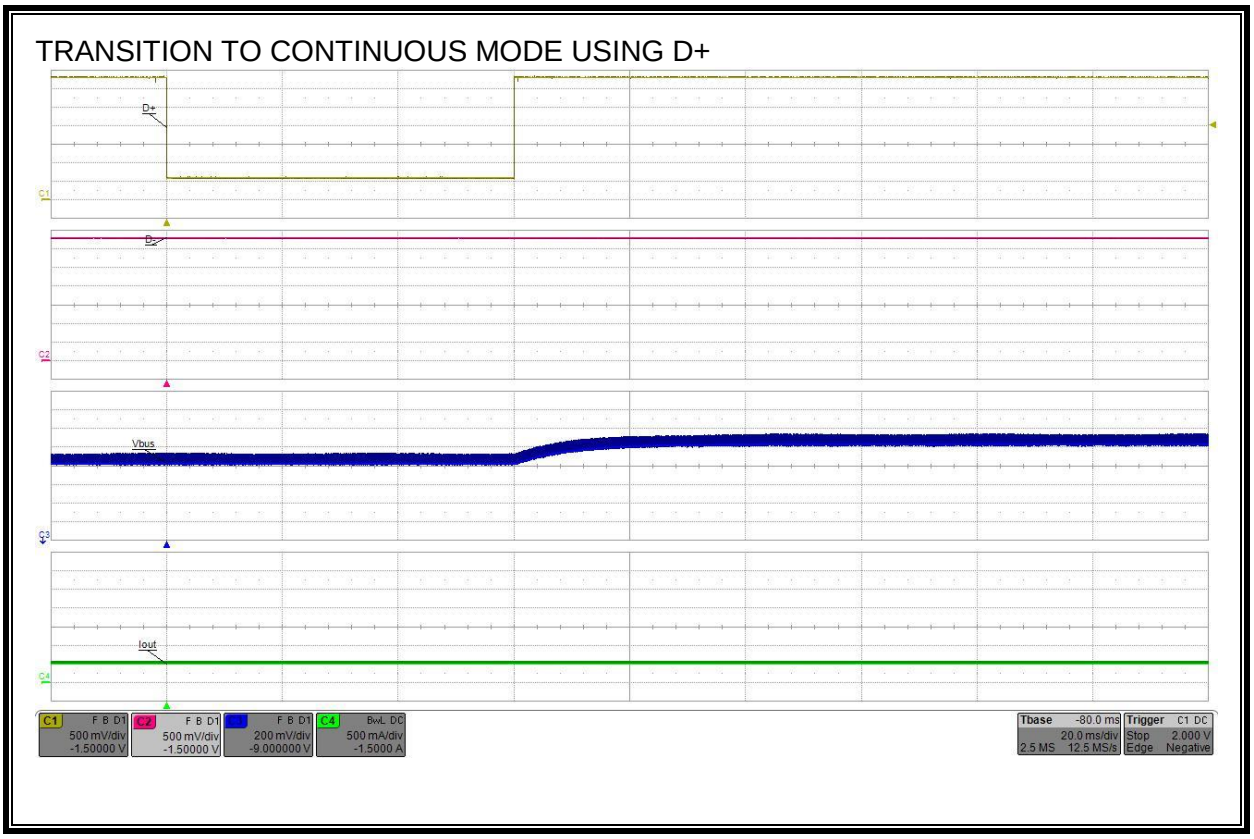
7.6. Continuous Mode Portable Device Request Recognition

7.6.1. Upper Bound of Tglitch_mode_change

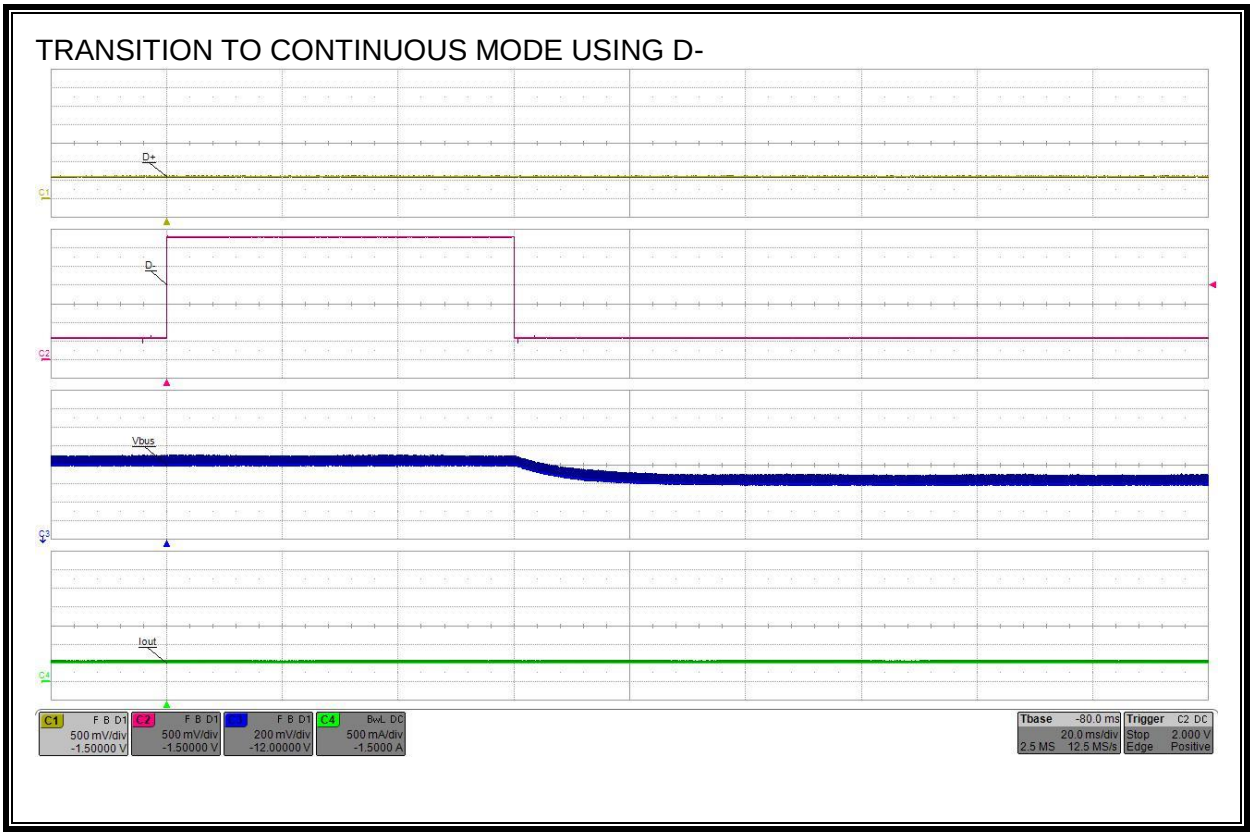
LIMITS AND RESULTS

Charger Transition	Observation of Vbus	Pass/Fail
To Continuous Mode using D+ Pulse	Increments	PASS
To Continuous Mode using D- Pulse	Decrements	PASS

WAVEFORM FOR TRANSITION USING D+



WAVEFORM FOR TRANSITION USING D-



7.6.2. Tv_cont_change & Vbus_cont_step at Upper Bound of D-Tglitch_cont_change

Tv_cont_change LIMITS AND RESULTS

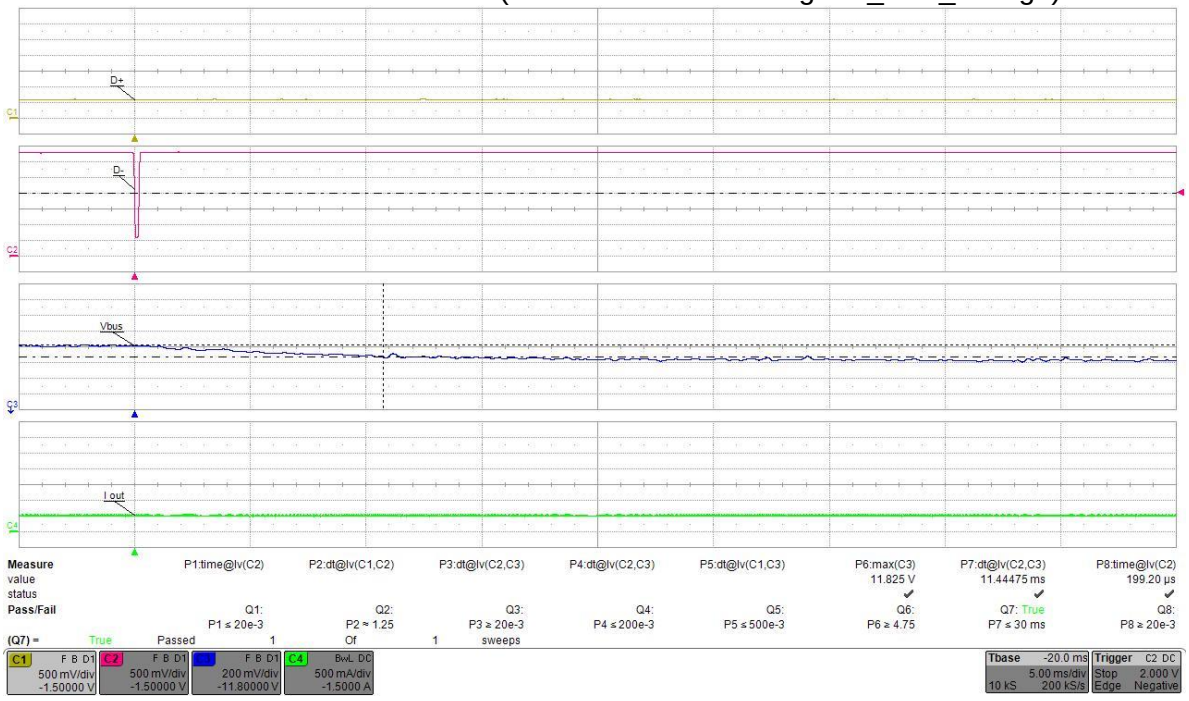
Vbus Transition	Time from leading edge of request to completion of Vbus transition (ms)	Maximum Limit (ms)	Pass/Fail
11.8 V to 11.6 V	11.44	30.0	PASS

Vbus_cont_step LIMITS AND RESULTS

Vbus Transition	Starting Voltage (V)	Ending Voltage (V)	Delta Voltage (V)	Minumum Delta (V)	Maximum Delta (V)	Pass/Fail
11.8 V to 11.6 V	11.817	11.632	0.185	0.150	0.250	PASS

DECREMENT WAVEFORM

DECREMENT USING 200 us PULSE (UPPER BOUND OF Tglitch_cont_change)



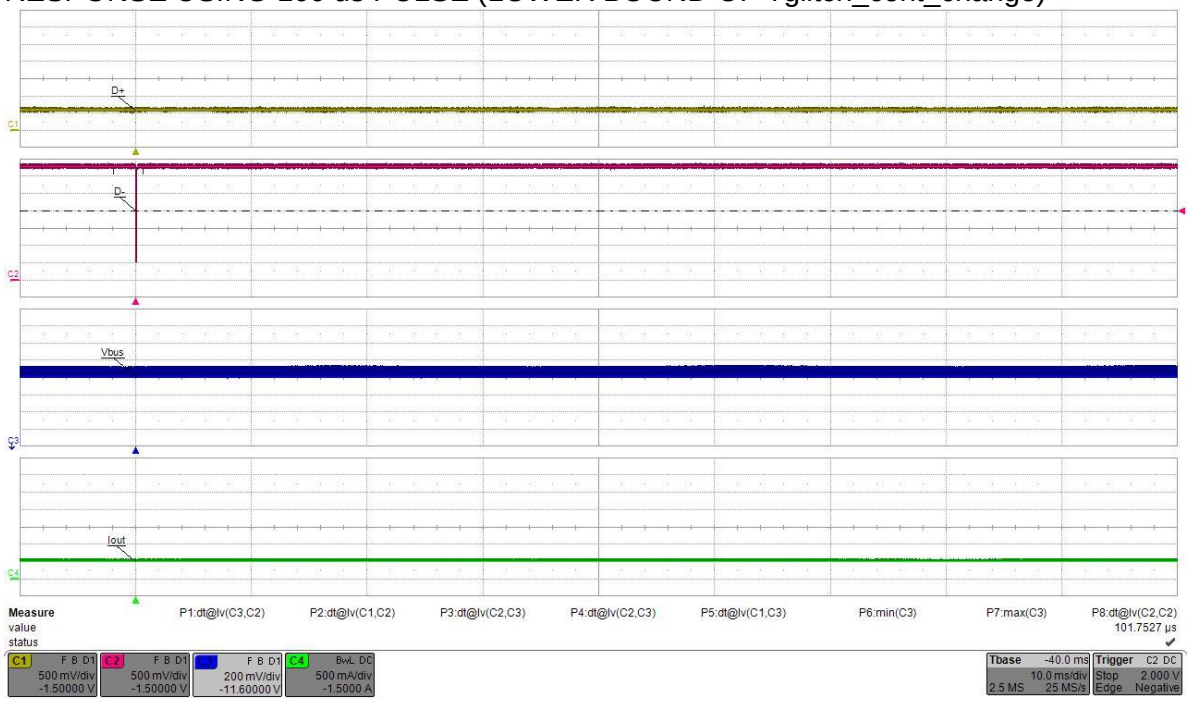
7.6.3. Lower Bound of D- Tglitch_cont_change

LIMITS AND RESULTS

D+ / D- Command	Observation of Vbus	Pass/Fail
Attempt to Decrement using D- Pulse Width < Minimum Tglitch_cont_change	Vbus does not Change	PASS

WAVEFORMS

RESPONSE USING 100 us PULSE (LOWER BOUND OF Tglitch_cont_change)

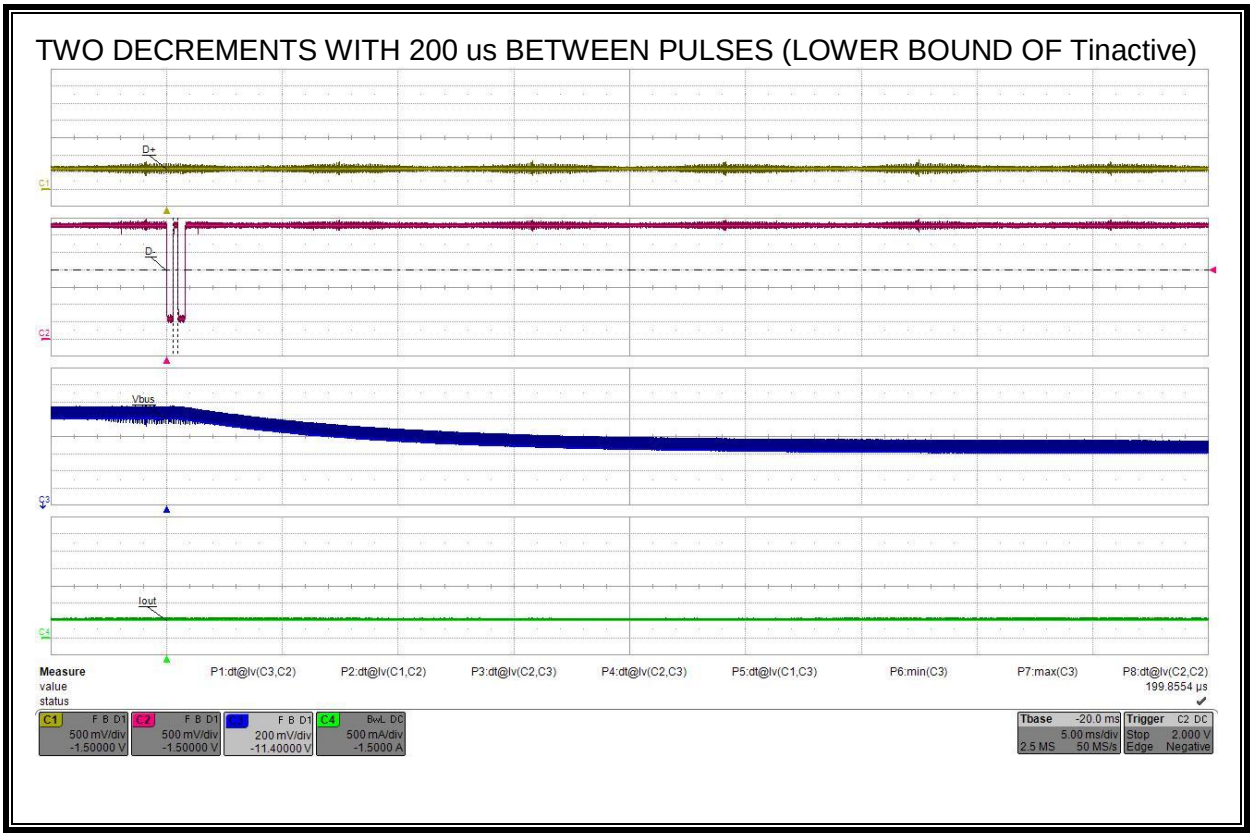


7.6.4. Lower Bound of D- Tinactive

LIMITS AND RESULTS

D+ / D- Command	Observation of Vbus	Pass/Fail
Two Decrement Pulses with minimum Tinactive timing	Vbus Decrements Twice	PASS

DECREMENT WAVEFORM



7.6.5. Tv_cont_change & Vbus_cont_step at Upper Bound of D+ Tglitch_cont_change

Tv_cont_change LIMITS AND RESULTS

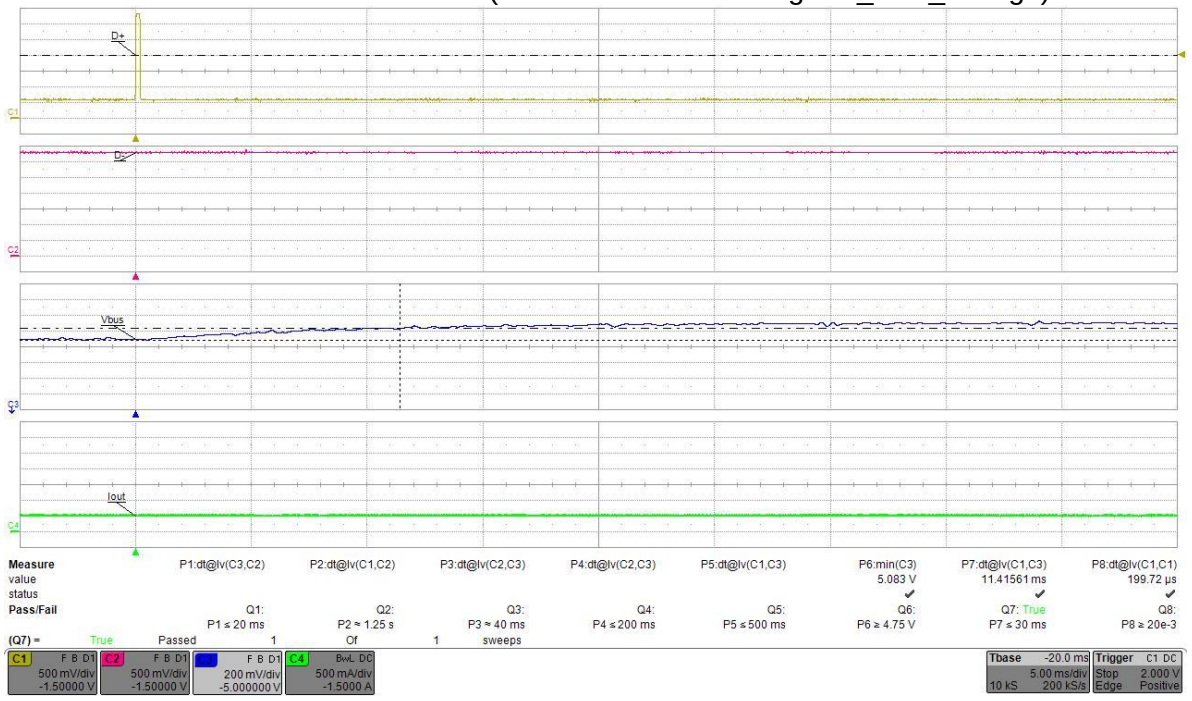
Vbus Transition	Time from leading edge of request to completion of Vbus transition (ms)	Maximum Limit (ms)	Pass/Fail
5.0 V to 5.2 V	11.42	30.0	PASS

Vbus_cont_step LIMITS AND RESULTS

Vbus Transition	Starting Voltage (V)	Ending Voltage (V)	Delta Voltage (V)	Minumum Delta (V)	Maximum Delta (V)	Pass/Fail
5.0 V to 5.2 V	5.100	5.304	0.204	0.150	0.250	PASS

INCREMENT WAVEFORM

INCREMENT USING 200 us PULSE (UPPER BOUND OF Tglitch_cont_change)

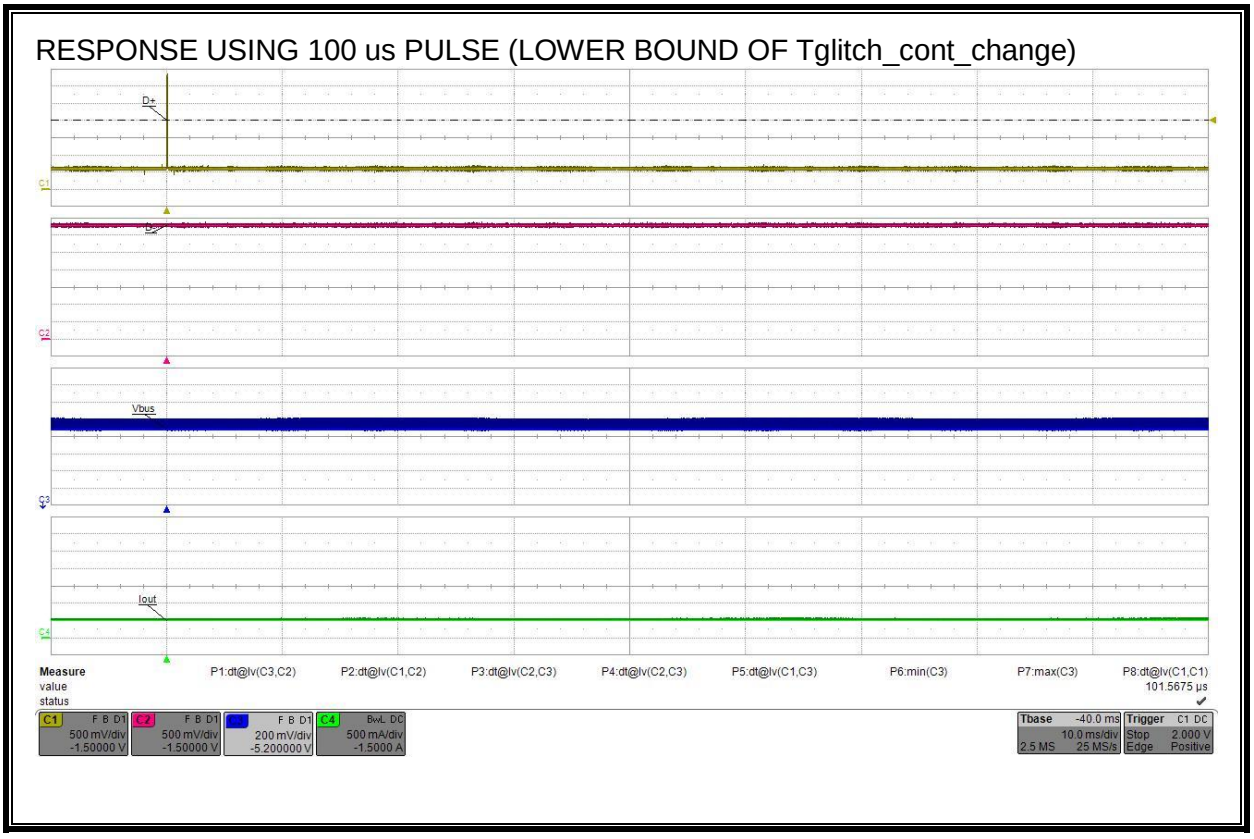


7.6.6. Lower Bound of D+ Tglitch_cont_change

LIMITS AND RESULTS

D+ / D- Command	Observation of Vbus	Pass/Fail
Attempt to Increment using D+ Pulse Width < Minimum Tglitch_cont_change	Vbus does not Change	PASS

WAVEFORMS

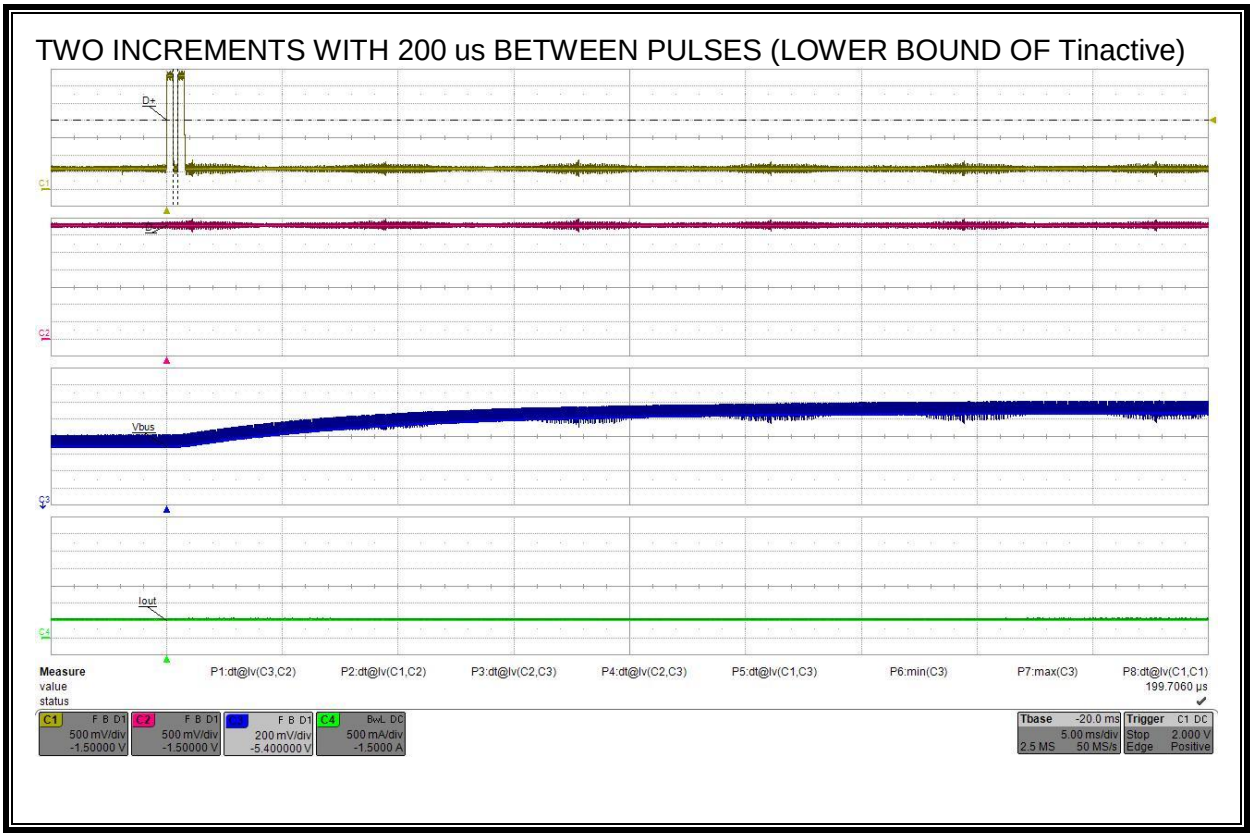


7.6.7. Lower Bound of D+ Tinactive

LIMITS AND RESULTS

D+ / D- Command	Observation of Vbus	Pass/Fail
Two Increment Pulses with minimum Tinactive timing	Vbus Increments Twice	PASS

INCREMENT WAVEFORM



7.6.8. Cumulative Tolerance of Vbus_cont_step

CUMULATIVE Vbus,cont,step LIMITS AND RESULTS

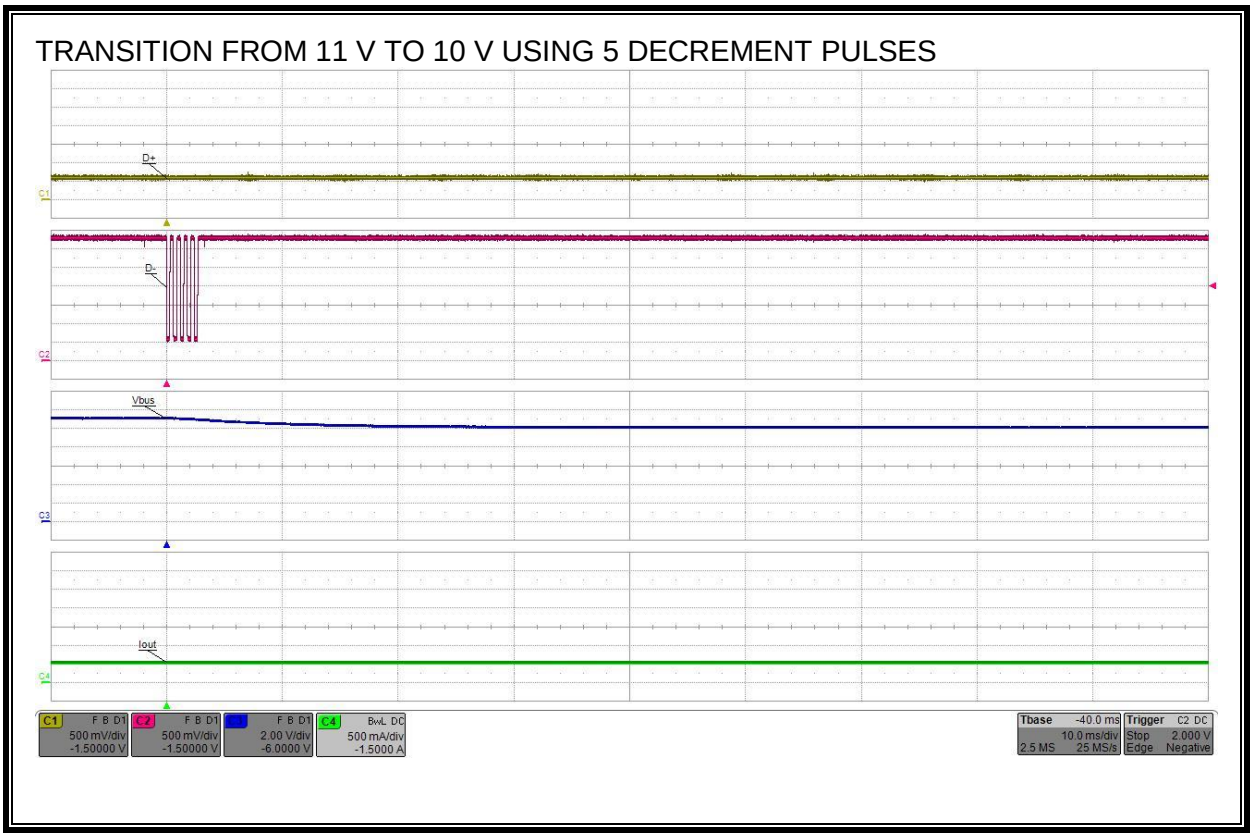
Requirement: Max. Tv_cont_change (30 ms) between the rising/falling edge of last pulse and the stable Vbus

Vbus Transition	Starting Voltage (V)	Ending Voltage (V)	Delta Voltage (V)	Minumum Delta (V)	Maximum Delta (V)	Pass/Fail
5 V to 11 V	5.10	11.02	5.92	4.50	7.50	PASS
11 V to 10 V	11.02	10.05	0.97	0.75	1.25	PASS

Vbus Transition	Observation of Vbus	Pass/Fail
5 V to 11 V	Vbus does not decrement during the process	PASS
11 V to 10 V	Vbus does not increment during the process	PASS

INCREMENT WAVEFORM

DECREMENT WAVEFORM



7.7. Transition from Continuous Mode to Fixed Mode

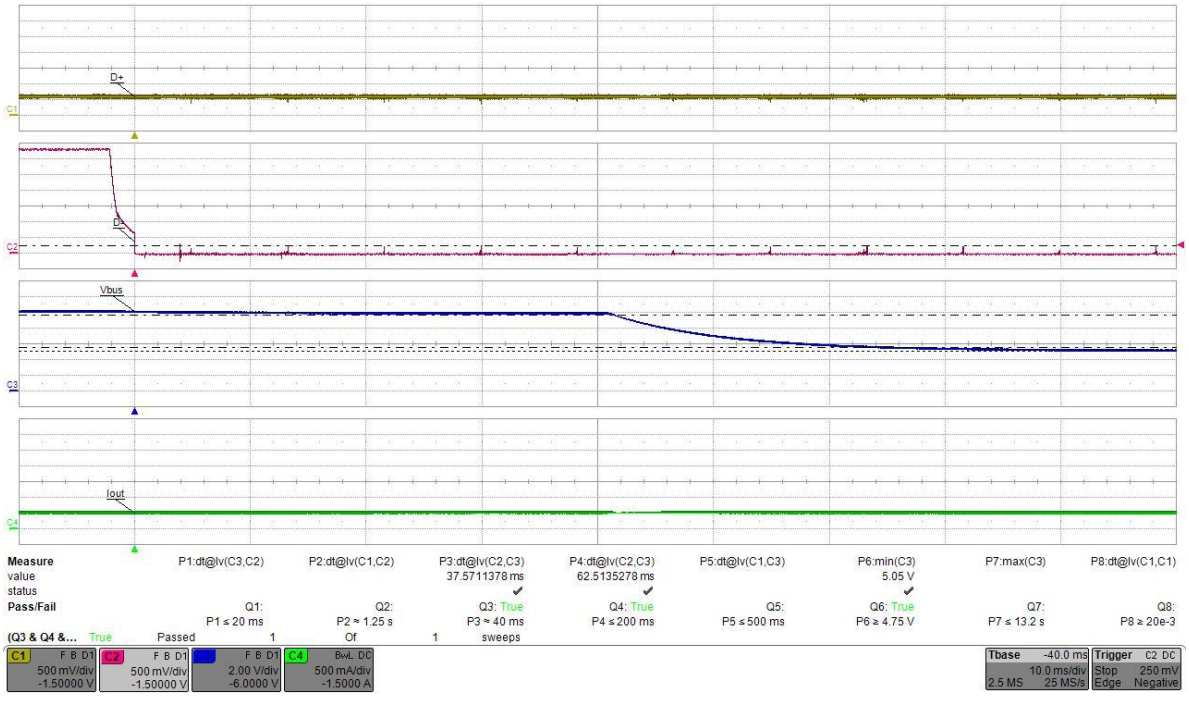
7.7.1. Transition from 10 V to 5 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- <= 0.25 V (Min Vdat_ref)	Vbus <= 9.6 V (Min Vbus_hv)	37.57	20	60	PASS
Tv_new_request	D- <= 0.25 V (Min Vdat_ref)	Vbus <= 5.5 V (Max Vbus_5v)	62.51		200	PASS

WAVEFORM AND MEASUREMENTS

TRANSITION FROM 10 V TO 5 V

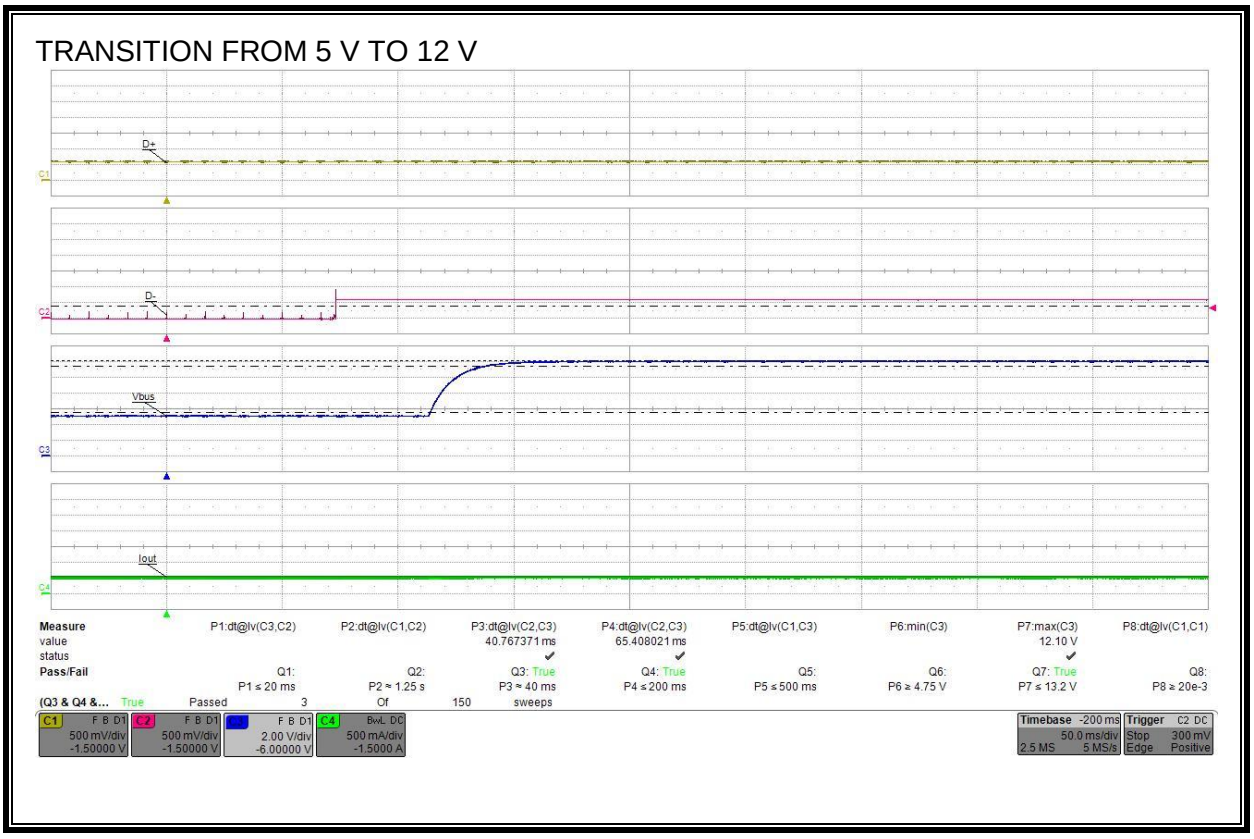


7.7.2. Transition from 5 V to 12 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 5.5 V (Max Vbus_5v)	40.77	20	60	PASS
Tv_new_request	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 11.4 V (Min Vbus_hv)	65.41		200	PASS

WAVEFORM AND MEASUREMENTS



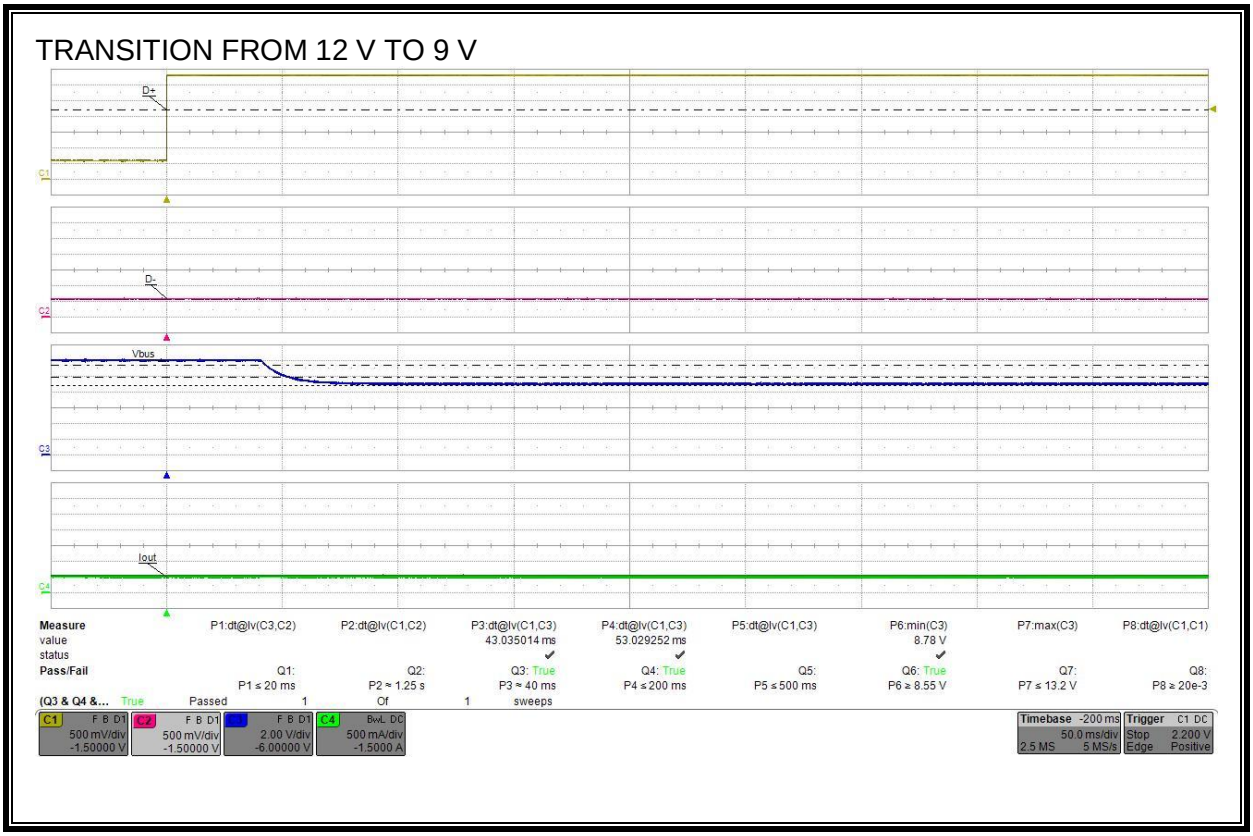
7.7.3. Transition from 12 V to 9 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 11.4 V (Min Vbus_hv)	43.04	20	60	PASS
Tv_new_request	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 9.9 V (Max Vbus_hv)	53.03		200	PASS

WAVEFORM AND MEASUREMENTS

TRANSITION FROM 12 V TO 9 V



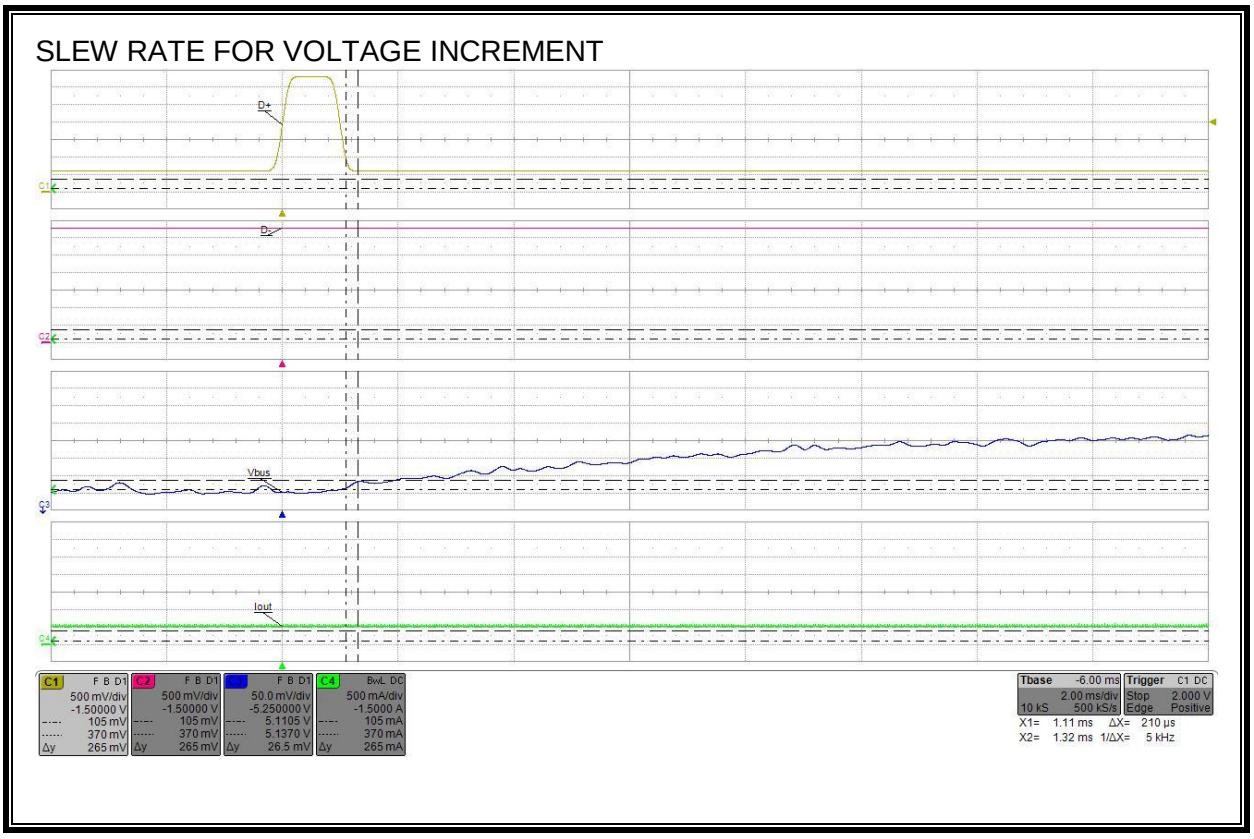
7.8. Operating Characteristics

7.8.1. Vslew_max

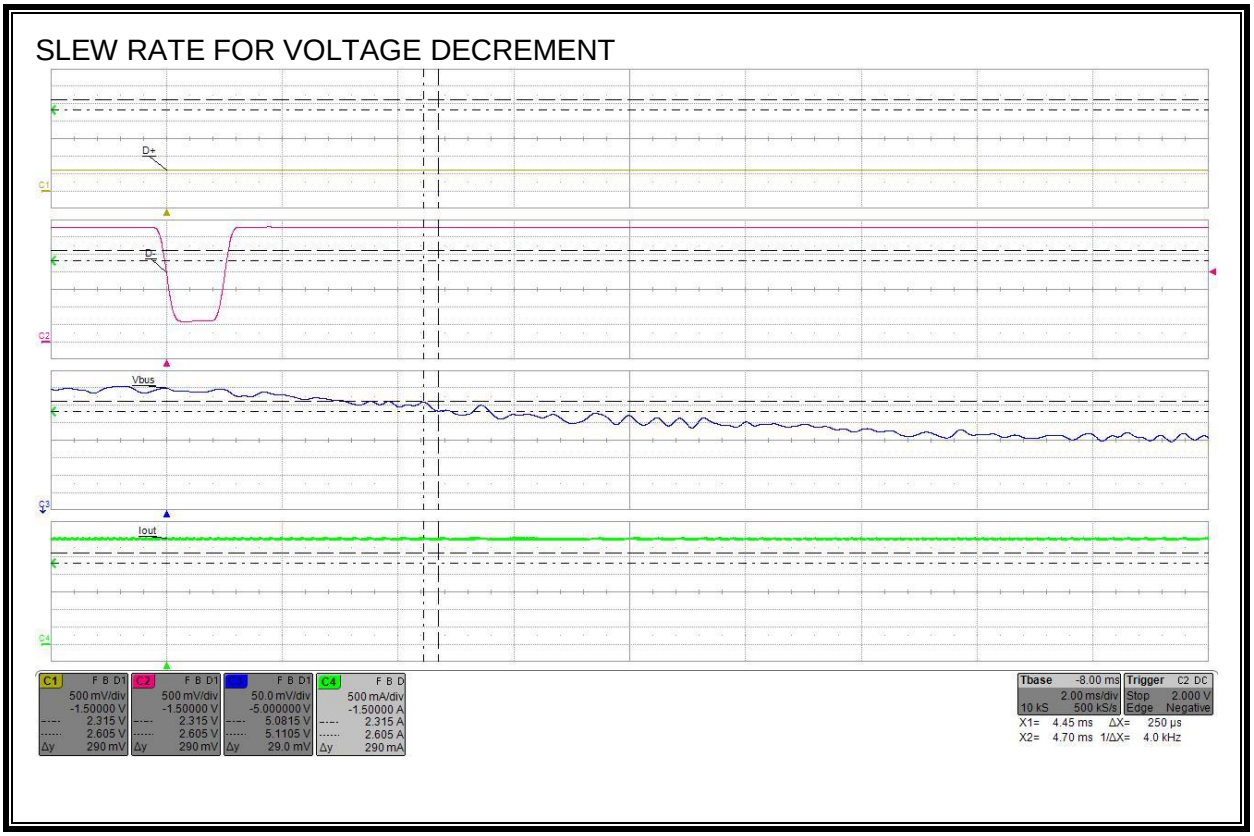
Vslew_max LIMITS AND RESULTS

Vbus Transition	Delta Voltage (mV)	Delta Time (usec)	Slew Rate (mV/usec)	Maximum Limit (mV/usec)	Pass/Fail
5.0 V to 5.2 V with 500 mA Load	26.500	210.000	0.126	30	PASS
5.2 V to 5.0 V with 3 A Load	29.000	250.000	0.116	30	PASS

WAVEFORM FOR INCREMENTING SLEW RATE



WAVEFORM FOR DECREMENTING SLEW RATE



7.8.2. Minimum Vbus_cont_range

Minimum Vbus_cont_range LIMITS AND RESULTS

Condition	Measured Value (V)	Minimum Limit (V)	Pass/Fail (Measured value must be <= Minimum Limit)
Current = 0.2 A	3.731	3.80	PASS
Current = Max Rated (3 A)	3.589		

7.9. Power Profile

7.9.1. Load Point A & Minimum Pmax

LOAD POINT A LIMITS AND RESULTS

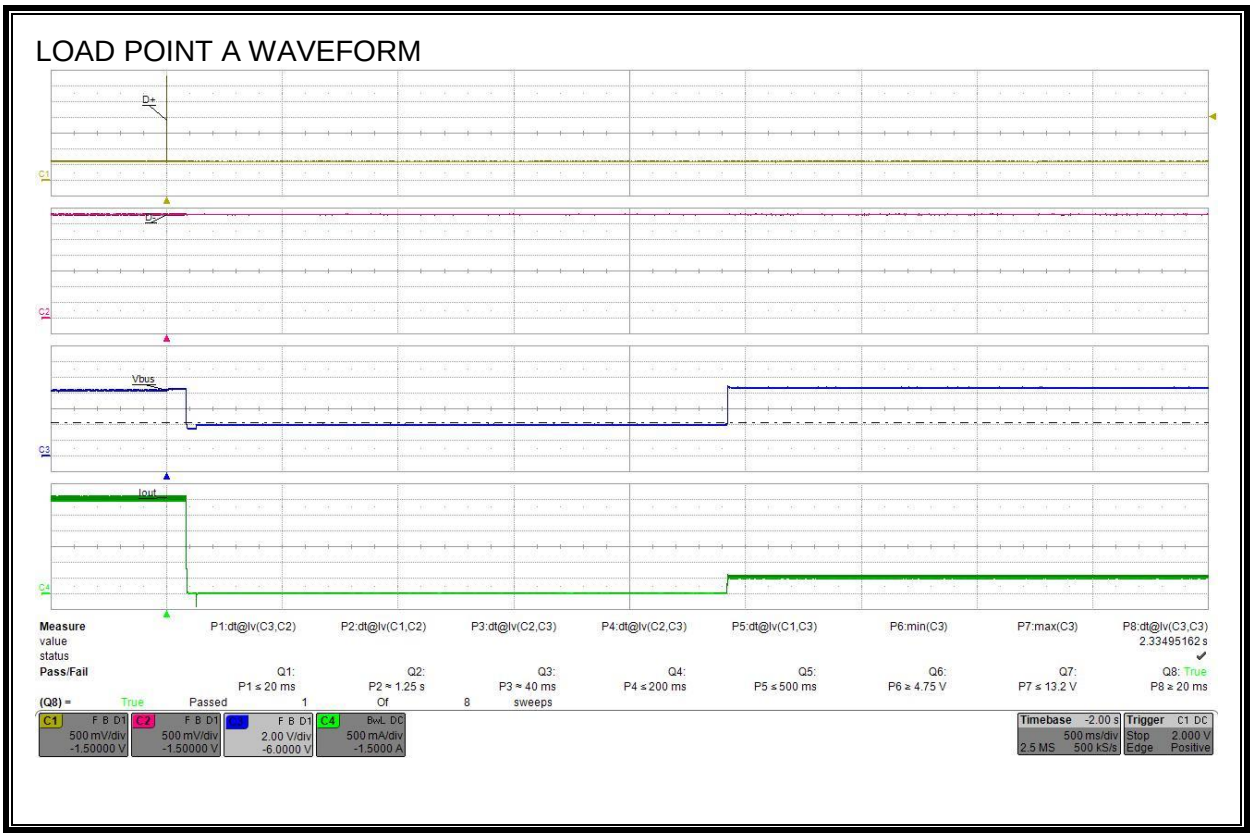
Measured Current (A)	Measured Load Point A Voltage Via Increment (V)	Minimum Voltage Limit (V)	Pass/Fail	Pmax (Watts)
3.00	8.360	6.00	PASS	25.08

7.9.2. Transition from Load Point A to Load Point B

Minimum Tglitch_uvlo LIMITS AND RESULTS

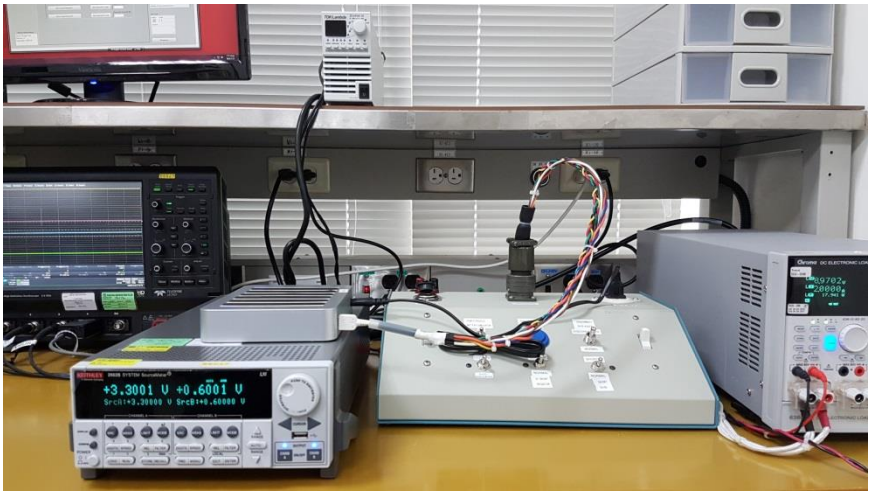
Parameter	Measured Value (ms)	Minimum Limit (ms)	Pass/Fail
Tglitch_uvlo	2334.95	20	PASS

VBUS REACHES LOAD POINT A



8. SETUP PHOTO

MEASUREMENT SETUP



END OF REPORT